AN2771
Application note

2x58 W/T8 or 2x36 W/T8 ballast demonstration board driven by L6585D

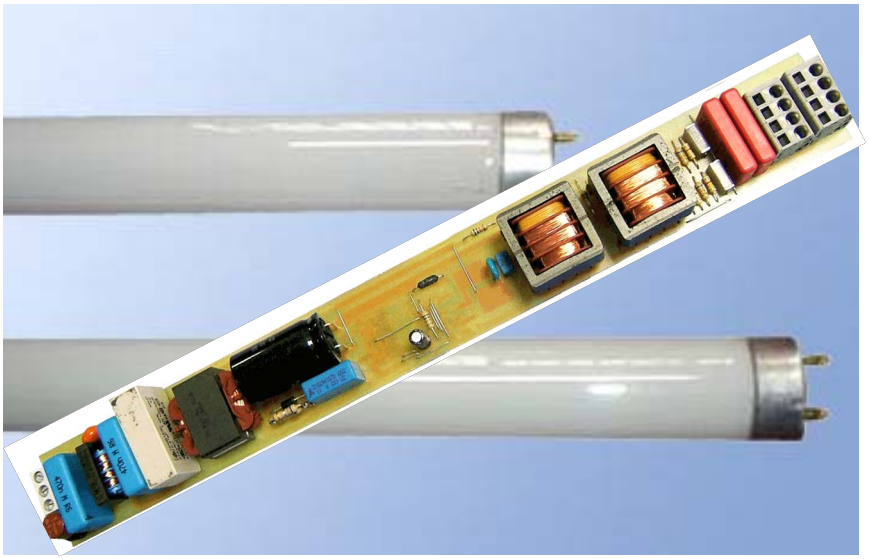
Introduction

This application note describes a demonstration board able to drive 2x58 W linear T8 fluorescent tubes. In addition, the modifications needed to adapt the same board for 2x36 W linear T8 fluorescent tubes are specified.

The ballast is controlled by STMicroelectronics' L6585D which integrates PFC and half-bridge control circuits, the relevant drivers, and the circuitry able to manage all lamp operating phases (preheating, ignition and run mode). Protections against primary failures (lamp disconnection, anti-capacitive mode, PFC overvoltage) are guaranteed and obtained with a minimum number of external components. After presenting the circuit description and design criteria, a short overview of the ballast performances is given.

Fluorescent lamps are driven more and more by electronic, rather than electromagnetic ballast, primarily because fluorescent lamps can produce around 20 % more light for the same input power when driven above 20 kHz instead of 50/60 Hz. Operation at this frequency also eliminates both light flickering (the response time of the discharge is too slow for the lamp to have a chance to extinguish during each cycle) and audible noise. An electronic ballast consumes less power and therefore dissipates less heat than an electromagnetic ballast. The energy saved can be estimated in the range of 20-25% for a given lamp power. Finally the electronic solution allows better control of the filament current and lamp voltage during preheating with the unquestionable benefit of increasing the mean lamp life.

Figure 1. 2x58W T8 ballast demonstration board



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1 Basis of half-bridge inverter topology

The half-bridge inverter operates in zero voltage switching (ZVS) resonant mode, to reduce the switching losses and the electromagnetic interference generated by the output wiring and the lamp. Voltage-fed series resonant half-bridge inverters are currently used for compact fluorescent lamp ballasts (CFL) and for many European tube lamp (TL) ballasts.

Generally, for lighting applications, considering the current preheating, it's possible to choose between two different topologies of the resonant circuit: capacitor-to-ground (*Figure 2*) or lamp-to-ground (*Figure 3*).

Figure 2. Electronic lamp ballast - capacitor-to-ground configuration

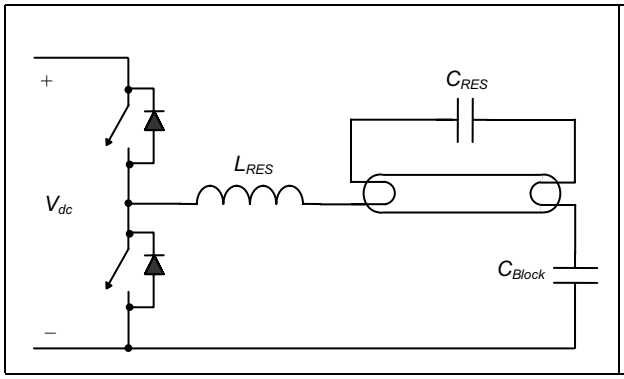
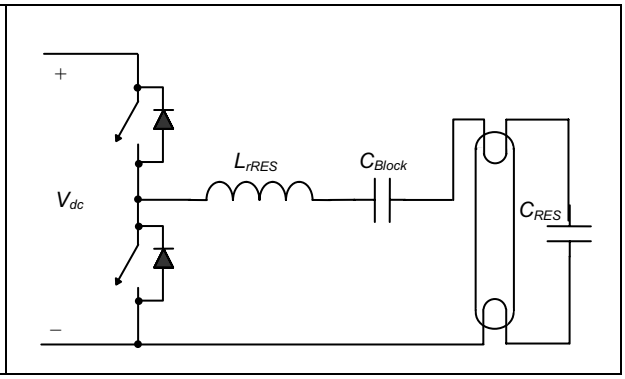


Figure 3. Electronic lamp ballast - lamp-to-ground configuration



In the design presented in this application note, a capacitor-to-ground configuration was used. For dual lamp ballast the lamps can be connected in series (*Figure 4*) or in parallel (*Figure 5*). In the system presented here, a parallel configuration was chosen for the following reasons:

- lower voltage stress on the ballast output stage components, on the wiring, and on the fixture sockets
- the resonant L and C associated with the lamps are less sensitive to component tolerances due to the lower operating lamp voltages compared to the series configuration
- better lamp control as it is possible to independently monitor both lamp operations

Figure 4. Dual lamp ballast series configuration

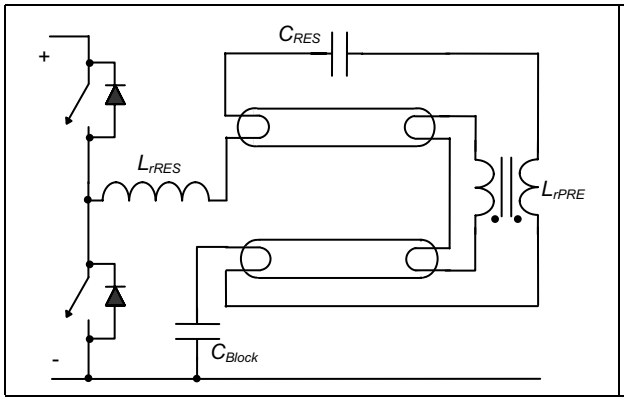
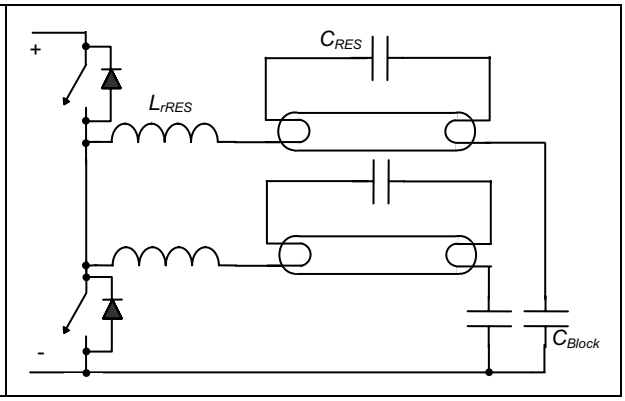


Figure 5. Dual lamp ballast parallel configuration



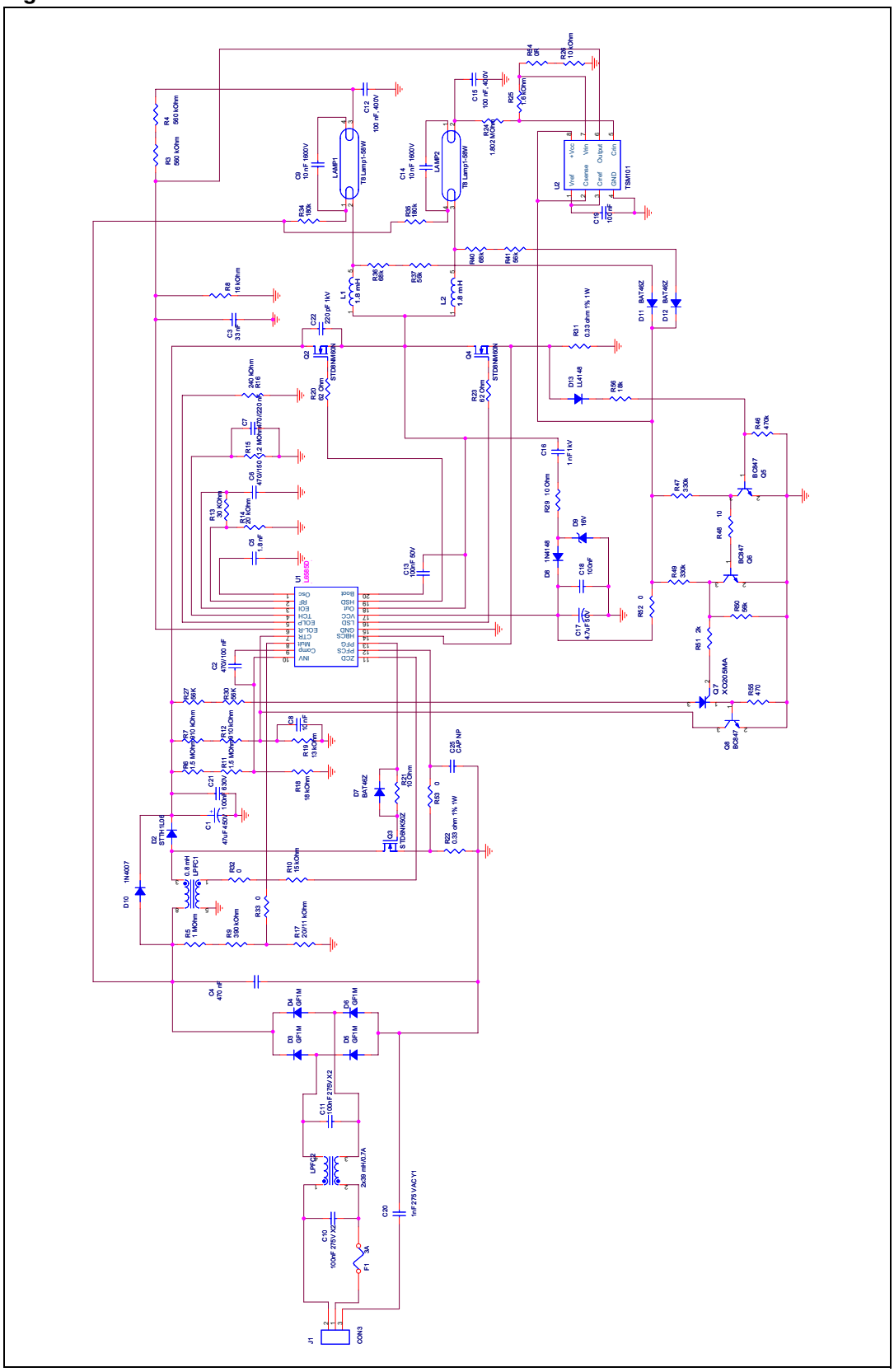
2 Main characteristics

The electrical specifications for the electronic lamp ballast are given in *Table 1* and the schematic for the 2x58 W T8 is presented in *Figure 6*. The ballast design procedure is detailed in the following section.

Table 1. Input and output parameters

Input parameters		
V_{IN}	Input voltage range	185 to 265 V_{RMS}
f_{line}	Line frequency	50/60 Hz
Tube lamp		
Number	2	
Type	T8 in parallel configuration	
Power	58 W or 36 W	
Target output parameters		
PF	Power factor	≈ 0.9
THD%	Total harmonic distortion	≤ 10
η %	Efficiency	≈ 90 %

Figure 6. Electrical schematic 2x58 W T8



3 Ballast design

The design of the major parts of the circuit is described in this section.

3.1 L6585D biasing circuitry (pin by pin)

Designed in high-voltage BCD offline technology, the L6585D embeds a PFC controller, a half-bridge controller, the relevant drivers and the logic necessary to build an electronic ballast.

- Pin 1 OSC is one of the two oscillator inputs. The value of the capacitor connected to ground defines the half-bridge switching frequency in each operating state. A value of 1.8 nF was chosen.
- Pin 2 RF. The component choice with oscillator capacitance defines the half-bridge switching frequency in each operating state. A resistor R_{14} connected to ground sets the run frequency while during preheating the switching frequency is set by the parallel of R_{14} with R_{13} connected between pins RF and EOI (short-circuit during preheating).

Choosing the following frequencies and ignition time:

$$f_{run} = 39\ kHz \qquad f_{pre} = 65\ kHz \qquad t_{ign} = 60\ ms$$

we can immediately calculate R_{14} with the following formula:

Equation 1

$$R_{14} = \frac{1.326}{f_{run} \cdot C_5} = 20\ k\Omega$$

and for the value of R_{13}:

Equation 2

$$R_{13} = \frac{1.326 \cdot R_{14}}{f_{pre} \cdot C_5 \cdot R_{14} - 1.41} = 30\ k\Omega$$

- Pin 3 EOI is a multifunction pin. During preheating the pin is internally shorted to ground by the logic, so the resistor (R_{PRE}//R_{RUN}) connected between the RF pin and ground sets the preheating switching frequency. During ignition pin EOI becomes high impedance. The ignition time is the time necessary for the pin voltage to exponentially rise from zero to 1.9 V. The growth is steered by the C_6* R_{13} time constant. As the value of R_{13} has already been calculated and t_{ign} at start is fixed, the value of C_6 is calculated by the following formula:

Equation 3

$$C_6 = \frac{t_{ign}}{3 \cdot R_{13}} = 666\ nF$$

The value C_6=620 nF was chosen. In order to have this value, two capacitors in parallel were mounted C_6=470//150 nF.

- Pin 4 TCH is the time counter and it is necessary to establish the preheating time and the protection intervention time (either overcurrent or EOL). To implement the time counter, a $R_{15}C_7$ parallel network is connected between this pin and ground. Choosing C_7=690 nF and t_{pre}=1 sec and considering the internal current generator I_{CH}=34 µA, we can calculate R_{15} as follows:

Equation 4

$$R_{15} = \frac{t_{pre} - \frac{C_7}{I_{CH}} \cdot 4.63}{C_7 \cdot \ln\frac{4.63}{1.5}} = 1.2\ M\Omega$$

- Pin 5 EOLP is a 2 V reference and allows programming the window comparator of pin 6 (EOLR) according to table 5 of the L6585D datasheet. Choosing a reference tracking with the CTR pin and a window voltage amplitude ± 220 mV, we chose R_{16}=240 kΩ.
- Pin 6 EOLR is the input of both the window comparator and a re-lamp comparator. Concerning the window comparator (choosing tracking with CTR pin), the center is the same voltage as the CTR pin so the resistive divider connected across the block capacitor (see C_{block} in *Figure 2*) is set such that under normal conditions:

Equation 5

$$V_{CTR} = V_{BUSpfc} \cdot \frac{R_{19}}{R_{19} + (R_7 + R_{12})}$$

$$V_{EOLR} = \frac{V_{BUSpfc}}{2} \cdot \frac{R_8}{R_8 + (R_3 + R_4)}$$

$$V_{EOLR} = V_{CTR} \Rightarrow \frac{(R_7 + R_{12})}{R_{19}} = 2 \cdot \frac{(R_3 + R_4)}{R_8} + 1$$

To determine the resistance values of (R_7+R_{12}), R_{19}, (R_3+R_4), R_8, decisions concerning pin 7 CTR are needed.

- Pin 7 CTR is a multifunction pin (PFC overvoltage, feedback disconnection, reference for EOL in case of tracking reading), connected to a resistive divider to the PFC output bus. Establishing the maximum PFC overvoltage (PFC output overshoot e.g. at startup) at $V_{OVPBUSpfc}$ = 480 V and considering that the correspondent threshold on the CTR pin must be V_{thrCTR} = 3.4 V, we can immediately calculate R_7+R_{12} = 1.82 MΩ and R_{19} = 13 kΩ. From *Equation 5*, fixing R_3+R_4 = 1120 kΩ, the following resistance value is obtained R_8 = 16 kΩ.
- Pin 8 MULT. Assuming a peak value of $V_{multpkMax}$ = 1.8 V (at VAC = 265 V) on the multiplier input (MULT, pin 8), the peak value at minimum line voltage is $V_{MULTpkmin}$ = 1.8 × 185/265 = 1.25 V which, multiplied by the maximum slope of the multiplier, 0.75, gives 0.94 V peak voltage on current sense (CS, pin 4). Since the linearity limit (1 V) is not exceeded, this is acceptable. Considering about 250 µA current for the divider, the lower resistor is 7.14 kΩ (20//11 kΩ). To establish the upper resistance value (referring to the PFC section of the L6585D datasheet), the ratio between Vmult and Vin for different input voltage must be evaluated:

Equation 6

$$V_{inMax} \Rightarrow \frac{R_{17}}{R_{17}+(R_5+R_9)} = \frac{V_{multPK\,max}}{\sqrt{2}\cdot V_{inMax}} = 4.8\cdot 10^{-3}$$

$$V_{inMin} \Rightarrow \frac{R_{17}}{R_{17}+(R_5+R_9)} = \frac{V_{multSlopeMax}}{\sqrt{2}\cdot V_{inMin}} = \frac{V_{CSclamp}}{\max slope}\frac{1}{\sqrt{2}\cdot V_{inMin}} = 5.1\cdot 10^{-3}$$

where:

- $V_{CSclamp}$ is the clamp value of the voltage current sense for L6585D
- max slope is the maximum slope of the multiplier characteristic family for L6585D
- $V_{multSlopeMax}$ is the maximum voltage in the mult pin with Vin=V_{inMin}

To work in the linear area of the multiplier characteristic family, the upper resistance choice is made considering the lowest of ratios calculated in *Equation 6* $\Rightarrow$ R_5+R_9=1.487 MΩ. R_5+R_9 = 1.390 MΩ was mounted.

- Pin 9 COMP is the output of the E/A and also one of the two inputs of the multiplier. The feedback compensation network, placed between this pin and INV (10), is simply a capacitor calculated as follows (considering R_6+R_{11} is the upper resistance of the voltage divider between the PFC bus and COMP pin):

Equation 7

$$C_2 = \frac{10}{2\cdot\pi\cdot(R_6+R_{11})} = 530\ nF$$

A value of C_2=560 nF was chosen.

- Pin 10 INV. To implement the voltage control loop, a resistive divider (*Figure 6*) is connected between the regulated output voltage V_{BUSpfc} = 420 V of the boost and the pin. The internal reference on the noninverting input of the E/A is 2.5 V, so R_6 and R_{11} (*Figure 6*) are then selected, establishing a max overvoltage $\Delta V_{OVPBUSpfc}$ = 60 V, as follows:

Equation 8

$$\frac{R_6+R_{11}}{R_{18}} = \frac{V_{BUSpfc}}{2.5} - 1$$

$$R_6+R_{11} = \frac{\Delta V_{OVPBUSpfc}}{I_{OVPth}} = 3\ M\Omega$$

$$\Rightarrow R_{18} = 17.964\ k\Omega \Rightarrow 18\ k\Omega$$

where I_{OVPth} = 20 µA is the threshold current flowing through the compensation network in case an abrupt load drop happens.

- Pin 11 ZCD is the input to the zero current detector circuit. The ZCD pin is connected to the auxiliary winding of the boost inductor through a limiting resistor. The ZCD circuit is negative-going edge-triggered: when the voltage on the pin falls below 0.7 V, the PWM latch is set and the MOSFET is turned on. To do so, however, the circuit must first be armed. Prior to falling below 0.7 V, the voltage on pin 11 must experience a positive-going edge exceeding 1.4 V (due to the MOSFET's turnoff). The maximum main-to-

auxiliary winding turn ratio, m, has to ensure that the voltage delivered to the pin during the MOSFET's OFF-time is sufficient to arm the ZCD circuit.

Then:

Equation 9

$$m \leq \frac{V_{BUSpfc} - \sqrt{2} \cdot V_{inRMS(max)}}{1.4} = 33.10$$

We chose m=10.

Considering the upper and lower clamp voltage of the ZCD pin, its minimum current sink current capability, according to the max and min voltage of the PFC bus, we can immediately calculate and choose R_{10} = 15 kΩ.

- Pin12 PFCS is the inverting input of the current sense comparator. As the voltage across the sense resistor (proportional to the instantaneous inductor current) crosses the threshold set by the multiplier output, the power MOSFET is turned off. Following the indication given in AN966, page 13, considering the max peak current absorbed by two lamps, it is possible to determine the following PFC sense resistor:

Equation 10

$$R_{22} \leq 340\ m\Omega$$

We chose R_{22}=330 mΩ with a power rating of 0.5 W.

Considering the clamp value voltage on this pin, $V_{CSclamp}$ = 1.16 V, it was possible to determine the maximum inductor current I_{Lmax} = 3.5 A.

- Pin13 PFG. To correctly drive the external MOSFET, a resistor R_{21}=10 Ω was used.
- Pin 14 HBCS. Establishing during ignition, for each lamp, a maximum current of I_{IGNmax} = 2.5 A and considering the HBCS threshold during ignition phase $V_{HBCS\text{-}ign}$ = 1.6 V, we can calculate $R_{senseHB}$=R_{31}:

Equation 11

$$R_{31} = \frac{V_{HBCS-ign}}{I_{IGNmax\,TOT}} = 0.32\ \Omega$$

We chose R31 = 0.33 Ω.

- Pin 15 GND: ground
- Pin 16 LSD. To correctly drive the external half-bridge low-side MOSFET, a resistor R_{23}=62 Ω was used.
- Pin 17 Vcc. This pin is externally connected to the startup circuit (by means of R_{34}, R_{35}, R_{37}, R_{40}, R_{41}) and to the self-supply circuit consisting of a charge pump composed of the net C_{16}, C_{17}, C_{18}, D_8, D_9, R_{29}.
- Pin 18 Out: high-side driver floating reference. This pin is connected close to the source of the high-side power MOSFET.
- Pin 19 HSD. To correctly drive the external half-bridge low-side MOSFET a resistor R_{20}=62 Ω was used.
- Pin 20 Boot. For the high-side section a C_{boot} = 100 nF was selected.

3.2 PFC power section design

Input capacitor

The input high-frequency filter capacitor C_4 has to attenuate the switching noise due to the high-frequency inductor current ripple. The worst conditions occur on the peak of the minimum rated input voltage V_{inmin} = 185 V where:

- the coefficient of maximum high frequency voltage ripple r = 0.05
- total system efficiency is possible, considering the minimum half-bridge switching frequency f_{swmin} = 39 kHz and the total output power P_{outTOT} = 2*58 = 116 W, to determine the input capacitor C_4 as follows:

Equation 12

$$C_4 = \frac{\frac{P_{outTOT}}{\eta \cdot V_{inmin}}}{2 \cdot \pi \cdot f_{swmin} \cdot V_{inmin} \cdot r} = 307\ nF$$

C_4=470 nF was chosen.

Output capacitor

The output bulk capacitor C_1 selection depends on the DC output voltage, the admitted overvoltage, the output power and the desired voltage ripple where:

- PFC output voltage V_{busPFC} = 420 V
- the coefficient of low-frequency (twice the mains frequency f_{min} = 50 Hz) voltage ripple r_1 = 0.05

We can calculate the bulk capacitor in *Equation 13*:

Equation 13

$$C_1 = \frac{\frac{P_{outTOT}}{V_{busPFC}}}{2\pi \cdot 2f_{main} \cdot V_{busPFC} \cdot r_1} = 21\,\mu F$$

To have the smallest ripple and good reliability, we chose capacitor C_1 =47 µF, 450 V.

Boost inductor

The inductance L_{pfc} is usually determined so that the minimum switching frequency $f_{min\ pfc}$ is greater than the maximum frequency of the internal starter in order to ensure a correct TM operation. Considering the minimum suggested value for the PFC section $f_{min\ pfc}$ = 20 kHz and that it can occur at the either the maximum $V_{inrmsMax}$ = 265 V or the minimum $V_{inrmsMin}$ = 185 V mains voltage, the inductor value is defined by:

Equation 14

$$L_{pfc} = \frac{V_{inrms}^2 \cdot \left(V_{busPFC} - \sqrt{2} \cdot V_{inrms}\right)}{2 \cdot f_{minpfc} \cdot \frac{P_{out}}{\eta} \cdot V_{busPFC}}$$

To obtain a margin from $f_{min\ pfc}$ we chose f_{pfc} = 33 kHz. In this condition the lower value for the inductor is determined by $V_{inrms} = V_{inrmsMax}$ and L_{pfc} = 0.8 mH with, as previously stated in the PFCS pin description, a maximum current I_{Lmax} = 3.5 A.

Power MOSFET

The choice of the MOSFET concerns mainly its $R_{DS(on)}$, which depends on the output power, and its breakdown voltage. This last voltage is fixed just by the output voltage V_{buspfc} = 420 V, plus the overvoltage ΔV_{OVPpfc} = 60 V allowed and a safety margin.

The MOSFET's power dissipation depends on the conduction and switching losses. Establishing maximum total power losses $P_{lossesAdm}$ = 1% and P_{outTOT} = 1.16 W, it is easy to verify that in choosing SuperMesh power MOSFET STD6NK50Z, the estimated total MOSFET power losses, in the worst case, is about $P_{lossesEst}$ = 0.6 W, so this choice was the definitive one.

Boost diode

The boost freewheeling diode is a fast recovery one. The breakdown voltage is fixed with the same criterion as the MOSFET. The values of its DC and RMS current, which are needed to choose the current rating of the diode, are given as follows:

Equation 15

$$I_{D2dc} = \frac{P_{outTOT}}{V_{BUSpfc}} = 0.276\ A$$

$$I_{D2rms} = 2\sqrt{2} \cdot I_{rms} \cdot \sqrt{\frac{4\sqrt{2}}{9\pi} \cdot \frac{V_{inrms}}{V_{BUSpfc}}} = 0.6\ A$$

Since the PFC works in transition mode, the Turbo 2 Ultrafast high-voltage rectifier STTH1L06 was selected.

3.3 Half-bridge inverter design

Concerning the resonant circuit design, according the criteria described in AN993 section 5, we chose the following:

- $$L_{res} = L_1 = L_2 = 1.8\ mH$$
- $$C_{res} = C_9 = C_{14} = 10\ nF / 1600\ V$$
- $$C_{block} = C_{12} = C_{15} = 100\ nF / 400\ V$$

The P-Mos selection in the half-bridge section is performed mainly considering the max power losses admitted on each switch $P_{lossesAdm1}$ = 0.5% $P_{outTOT} \cong$ 0.6 W and the rms current through it IrmsMOS $\cong$ 0.6 A. Concerning half-bridge devices, using the second generation MDmesh Power MOSFET STD8NM60N, the estimated power losses in it result in $P_{lossesEstHB} \cong$ 0.468 W.

3.4 Symmetrical and asymmetrical EOL protection: improvements

As previously stated, the L6585D includes two functions concerning EOL protections which are summarized as follows:

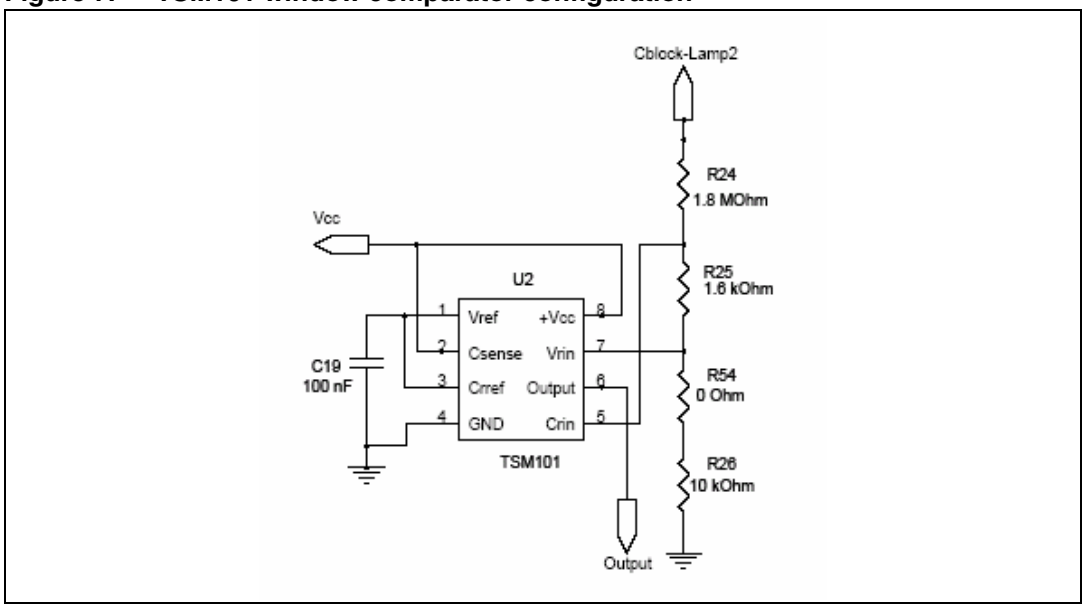
a) The first function has been designed to detect the ageing of the lamp with particular attention to the effect appearing as asymmetric rectification. The idea is to measure the variation of the DC component of the lamp voltage that can be either positive or negative. A window comparator has been introduced (centered around Vref with amplitude "V_w") that triggers when the EOL-R voltage is higher than V_{set}+ V_w/2 or lower than Vref- V_w/2. This kind of protection is compliant to the two standard ballast configurations (lamp-to-ground and block capacitor-to-ground).

b) Concerning the second function, as soon as a fault due to broken lamp in ignition mode (1.6 V threshold crossing) or a symmetrical EOL in run mode (0.9 V threshold crossing) triggers the TCH timer, the frequency control starts. When the timer ends, the current is monitored on the HBCS pin at the first cycle. In both conditions if the HBCS threshold is still crossed, the oscillator stops, the chip enters low-consumption mode /shutdown mode and this condition is latched until the mains supply is removed or re-lamp is detected.

The following improvements in the protection functions have been implemented:

– The asymmetric rectification protection, described above, was implemented to monitor the status of only one lamp. To protect the second lamp with the same criteria (voltage window comparator) as the first one, a voltage and current control TSM101 in the configuration shown in *Figure 7* was used. With this circuit it was possible to obtain the asymmetric rectification protection in a reliable and independent manner for each lamp.

Figure 7. TSM101 window comparator configuration



The design criteria for TSM101 in window comparator configuration is described in the following paragraphs. By means of a voltage divider R_{24}, R_{25}, R_{54}+R_{26}, from the block

capacitor of the second lamp, TSM101 checks that the average voltage value on the capacitor is V_{AVE} = 210 V.

Considering that the voltage window used for the first lamp is $\Delta V_{window1}$ = 2*220 mV ≅ 15%V_{CTR}, for the second lamp a similar percent voltage window $\Delta V_{window2} \cong 15\%V_{AVE}$ = 31 V was chosen. Establishing the second voltage window and considering that the voltage reference in TSM101 is V_{ref} = 1.24 V, it is easy to calculate the resistance value of the voltage divider mentioned in the previous paragraph (presuming, in normal conditions, an absorbed current in it of $I_{Vdivider} \cong 116\ \mu A$) as follows:

Equation 16

$$R_{tot} = R_{24} + R_{25} + R_{54} + R_{26} = \frac{V_{AVE}}{I_{Vdivider}} = 1.81\,M\Omega$$

$$R_{54} + R_{26} = V_{ref} \cdot \frac{R_{tot}}{V_{AVE} + \frac{\Delta V_{window2}}{2}} = 9954\Omega \Rightarrow R_{54} + R_{26} = 10\ k\Omega$$

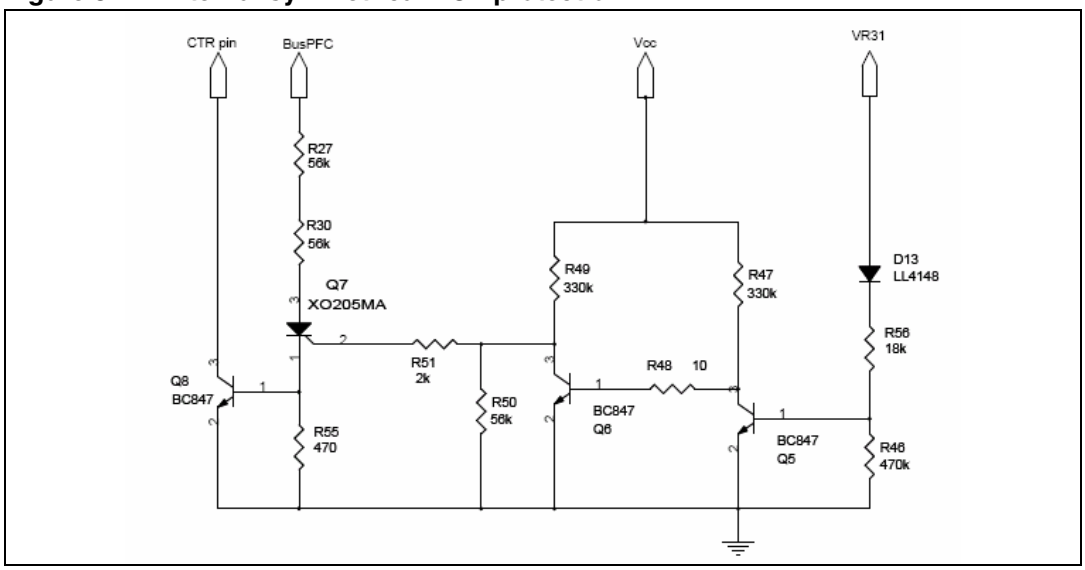
$$R_{25} = \frac{V_{ref} - (R_{54} + R_{26}) \cdot \frac{\left(V_{AVE} - \frac{\Delta V_{window2}}{2}\right)}{R_{tot}}}{\frac{\left(V_{AVE} - \frac{\Delta V_{window2}}{2}\right)}{R_{tot}}} = 1540\Omega \Rightarrow R_{25} = 1.6\ k\Omega$$

$$R_{24} = R_{tot} - (R_{25} + R_{54} + R_{26}) = 1.798\ M\Omega \Rightarrow 1.8\ M\Omega$$

– The symmetrical EOL protection described in paragraph *b* of this section was improved because for a two-lamp application an event such as the breaking of one lamp and the ignition of the other one may not activate the embedded device protection quickly enough.

To avoid this type of issue and in order to increase the reliability of the protection, an external circuit as shown in *Figure 8* was implemented.

Figure 8. External symmetrical EOL protection



This circuit (considering that it is possible to latch the device maintaining the CTR pin to zero voltage), by means of an inverting logic made by Q_5 and Q_6, is activated by the voltage on the half-bridge current sense resistor V_{R31}. Overcoming a fixed voltage threshold on the HB current sense, the X0205MA SCR is activated which consequently activates Q_8 and causes the CTR pin to go down to zero voltage. The device is latched until the main supply is removed.

4 Experimental results

The schematic of the tested board is shown in *Figure 6* . The board was first tested in terms of efficiency, power factor, total harmonic distortion and thermal behavior for the input voltage range. *Table 2* and *Table 3* show the results obtained for testing during 45 minutes.

Table 2. 2x58 W T8 board performance

V_{IN} (V)	P_{IN} (W)	$P_{OUTlamp1}$ (W)	η	I_{IN} (A)	PF	THD (%)
185	115.5	52	0.90	0.645	0.995	7.9
230	112.5	52	0.92	0.515	0.992	8
265	113.5	52	0.91	0.455	0.988	10

All results obtained are very good. Efficiency is about 90%, the power factor corrector is constantly 0.99, and THD is about 8%.

Table 3. 2x58 W T8 thermal results of critical system components

V_{IN} (V)	Ambient temp (°C)	Temp $MOS_{LowSide}$ (°C)	Temp $MOS_{HighSide}$ (°C)	Temp MOS_{PFC} (°C)	Temp L6585D (°C)
185	23	71	79	58	49
230	23	71	79	47	47
265	23	71	78	44	47

Concerning thermal behavior, from the results given in *Table 3*, it is easy to deduce, considering the highest ambient temperature, that there is a good safety margin from the max junction temperature of the MOS.

Startup sequence

Figure 9 shows the startup sequence: the IC supply voltage V_{CC} reaches V_{CCon}, the half-bridge starts oscillating and starts the charge capacitor connected to TCH. When the voltage at the TCH pin reaches VCHP (4.63 V), the same capacitor is discharged following an exponential decrease steered by the time constant, which defines the preheating time.

During this time, the EOI pin is forced to ground and the switching frequency is set by the oscillator at the preheating value. When the voltage at the TCH pin drops down to 1.53 V, the EOI pin is exponentially charged according to a time constant that defines the ignition time. At the same time the TCH pin goes down to ground. During this phase the oscillator generates a reduction of the switching frequency. As the voltage at EOI exceeds 1.9 V, the chip enters run mode.

Figure 9. L6585 startup sequence

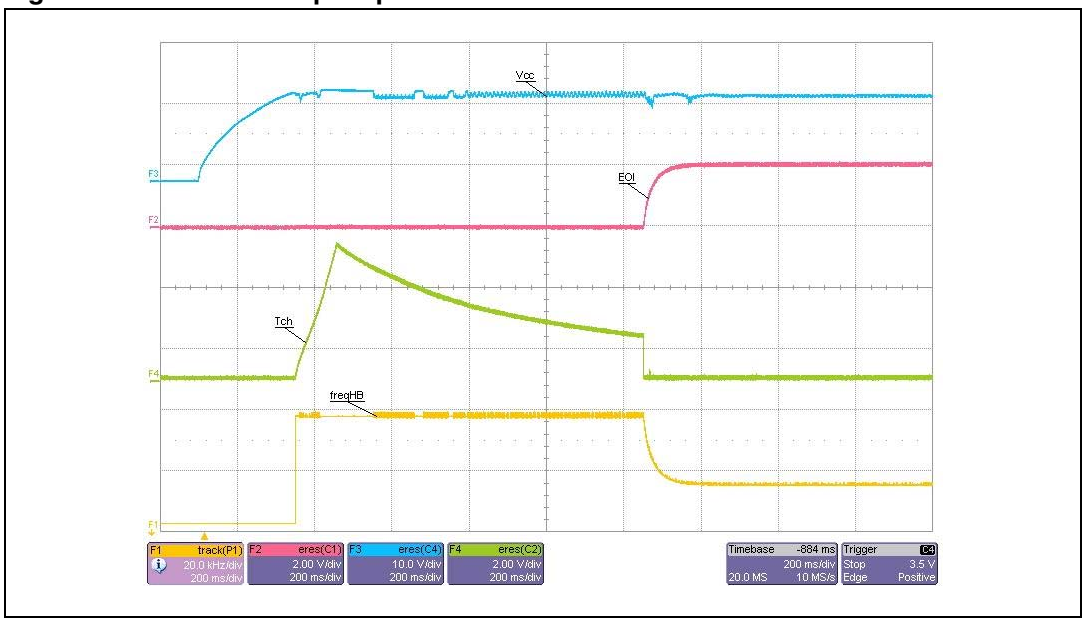

Vcc
EOI
Tch
freqHB
F1 track(P1) 20.0 kHz/div 200 ms/div
F2 eres(C1) 2.00 V/div 200 ms/div
F3 eres(C4) 10.0 V/div 200 ms/div
F4 eres(C2) 2.00 V/div 200 ms/div
Timebase -884 ms 200 ms/div 20.0 MS 10 MS/s
Trigger Stop 3.5 V Edge Positive

Figure 10 shows the lamp ignition phase. The voltage across it increases linearly as well as the current flowing through it.

Figure 10. One lamp ignition phase

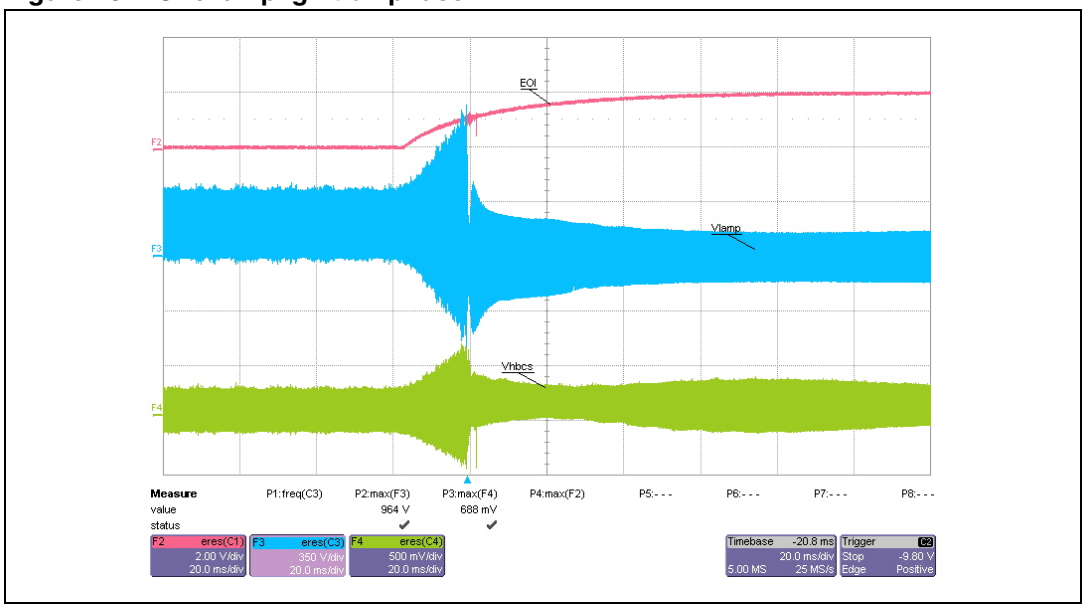


Figure 11. Low-side current in run mode

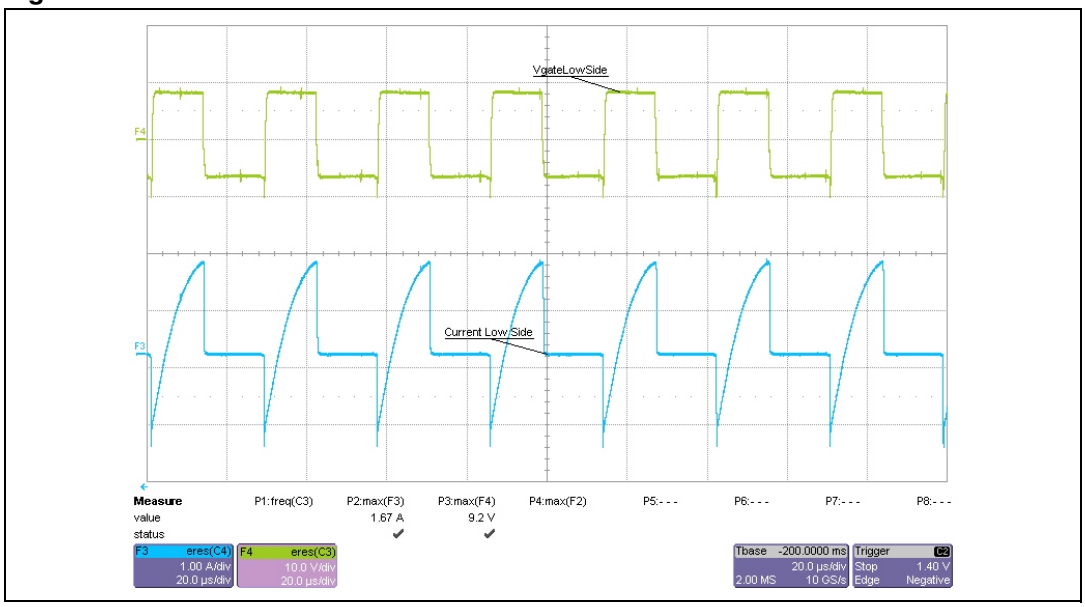
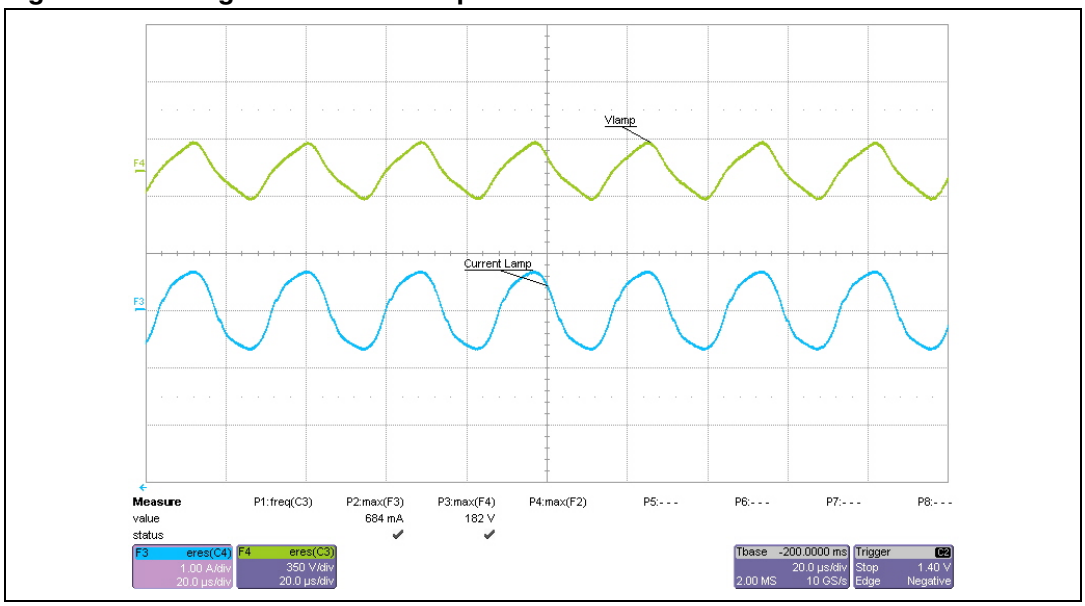


Figure 12. Voltage and current lamp in run mode



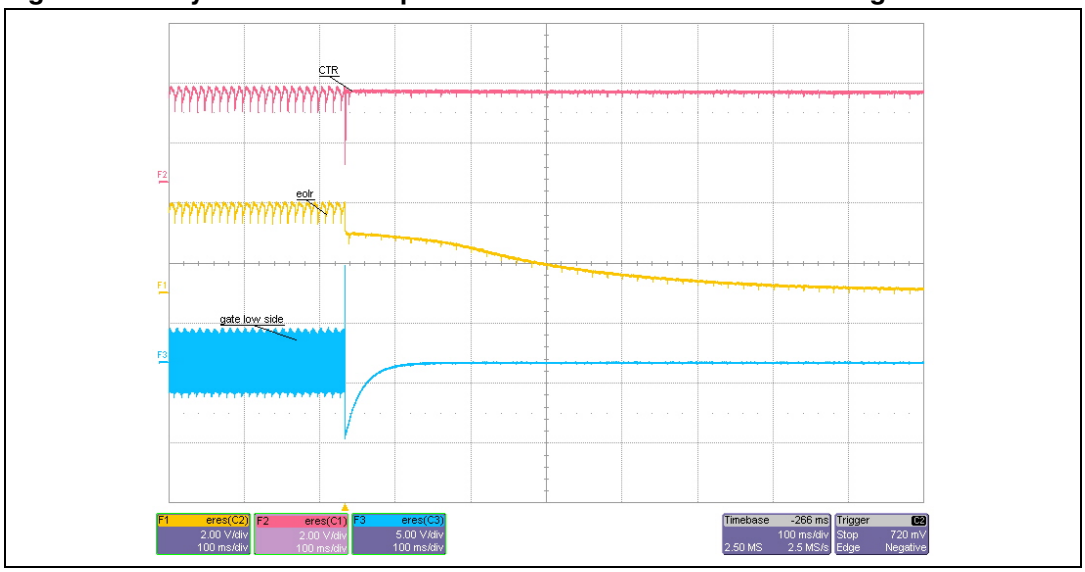
5 Protections

As previously stated in *Section 3.4*, due to the presence of two lamps, TSM101 must be added to implement the asymmetric EOL protection, and inverter logic with a SCR must be added to implement the symmetrical EOL protection. The following failures were simulated to test these:

- Cathode breaking in run mode
- Broken tube or failure to strike during ignition phase

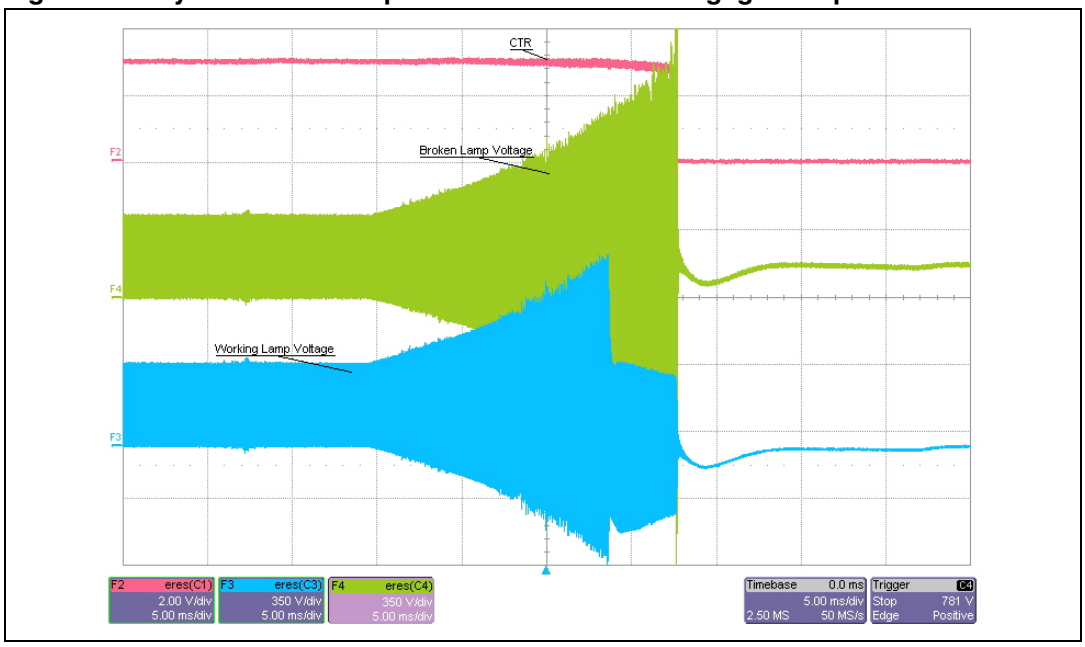
As shown in *Figure 13*, as soon as a cathode of one lamp is broken, the voltage on the EOLR pin goes out from the valid voltage window and the L6585D stops switching.

Figure 13. Asymmetrical EOL protection with broken cathode during run mode


CTR
eolr
gate low side
F1 eres(C2) 2.00 V/div 100 ms/div
F2 eres(C1) 2.00 V/div 100 ms/div
F3 eres(C3) 5.00 V/div 100 ms/div
Timebase -266 ms 100 ms/div 2.50 MS 2.5 MS/s
Trigger Stop 720 mV Edge Negative

When one of the two lamps is broken or the the gas inside is exhausted, during the ignition phase, as illustrated in *Figure 14*, the right lamp is ignited normally, but the voltage across the broken lamp rises up continually until an established threshold is exceeded that activates the SCR, by means of an inverter logic, and moves the CTR pin down to ground. In this condition the L6585D is latched.

Figure 14. Symmetrical EOL protection behavior during ignition phase



6 Conduction emissions test

Conducted emissions have been measured in neutral and line wires using peak detector and considering the limits for lighting applications i.e. EN55015. The measurements have been performed at 230 Vac line. The results are shown in *Figure 15* and *Figure 16*. Since the emission level is below both the quasi-peak and average limits with an acceptable margin, the power supply passes the precompliance test.

Figure 15. Conducted emissions at 230 Vac 50 Hz - line 1 peak detector

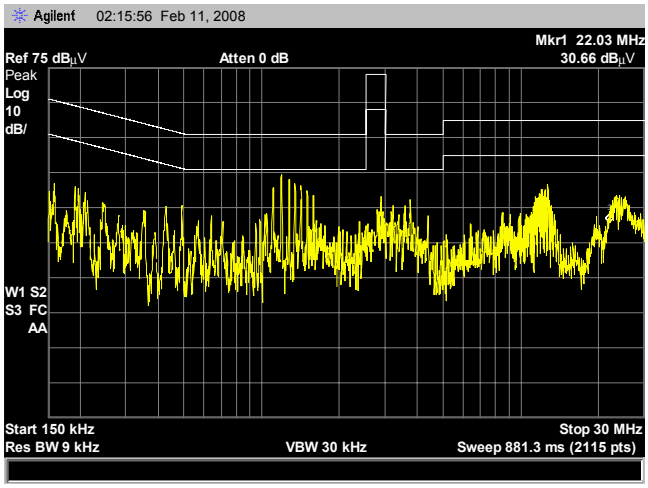
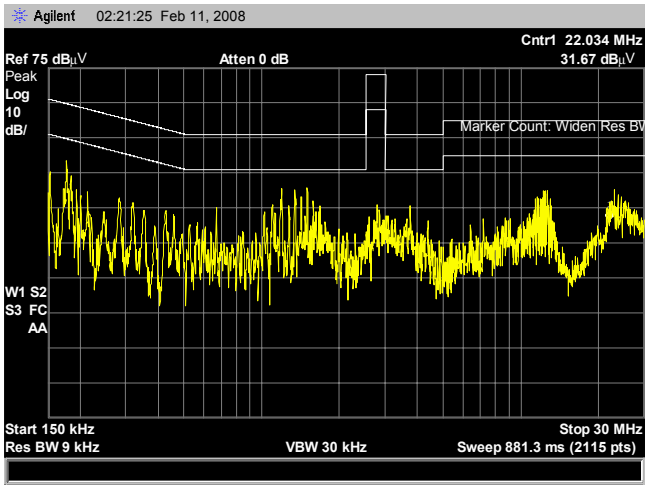


Figure 16. Conducted emissions at 230 Vac 50 Hz - line 2 peak detector



6.1 Adapting the design for a 2x36 W T8 electronic ballast

Using a developed design for 2x58 W T8 tubes, it was possible to do some simple adjustments to adapt the same design for 2x36 W T8 tubes. Using the same resonant

circuit, the adjustments concern only the operating frequencies of the lamp, setting the following ones at:

$$f_{run} = 49\ kHz \qquad f_{preh} = 65\ kHz$$

we can immediately calculate, by means of *Equation 1* and *Equation 2*, the following value resistances:

$$R_{14} = 15\ k\Omega \qquad R_{13} = 47\ k\Omega$$

In addition a new calibration for the symmetric end-of-life operation is needed, changing the following resistance to:

$$R_{56} = 75\ \Omega$$

Testing the board with these modifications the experimental results are given below in *Table 4*:

Table 4. 2x36W T8 board performance

V_{IN} (V)	P_{IN} (W)	$P_{OUTlamp1}$ (W)	η	I_{IN} (A)	PF	THD (%)
185	74	33	0.89	0.39	0.994	6.9
230	73.5	33	0.89	0.315	0.987	7.6
265	73.4	33	0.89	0.275	0.979	8.7

Table 5. Bill of material

Item	Qty	Ref.	Part/value	Tolerance (%)	Voltage - current	Watt	Technology information	Package footprint	Manu-facturer	Manufacturer code	RS/ distrelec /other code
1	1	C1	47 µF, 098 A	20%	450 V		Electrolytic capacitor		EPCOS	B43858C5476M 000	
2	1	C2	560 nF (470//100 nF)	5%	50 V		COG ceramic capacitor	SMD 0805			
3	1	C3	33 nF	5%	50 V		COG ceramic capacitor	SMD 0806			
4	1	C4	470 nF	10%	630 V		Polyester capacitor	Radial 22.5 mm lead spacing	EPCOS	B32523Q8474K 000	
5	1	C5	1.8 nF	5%	50 V		COG ceramic capacitor	SMD 0805			
6	1	C6	660 nF (470//150) nF- ceramic	5%	50 V		COG ceramic capacitor	SMD 0805			
7	1	C7	680 nF (470//220) nF-ceramic	5%	50 V		COG ceramic capacitor	SMD 0805			
8	1	C8	10 nF- ceramic-	5%	50 V		COG ceramic capacitor	SMD 0805			

Table 5. Bill of material (continued)

Item	Qty	Ref.	Part/value	Tolerance (%)	Voltage - current	Watt	Technology information	Package footprint	Manu-facturer	Manufacturer code	RS/ distrelec /other code
9	2	C9, C14	10 nF	5%	1600 V		Metallized polypropylene film capacitors	Radial 22.5mm lead spacing	EPCOS	B32653A1103J 000	
10	2	C10,C11	100 nF	10%	300 Vac		X2 polypropylene capacitor				RS: 441-9616
11	2	C12, C15	100 nF, 400 V-polyester-lead spacing 10mm	10%	400 V		Metallized polyester film capacitors	Radial 10mm lead spacing	EPCOS	B32561J6104K 000	
12	1	C13	100 nF-50V- 10%	10%	50 V		Ceramic capacitor	SMD 1206			
13	1	C16	1 nF	5%	630 V		Polypropylene capacitor	Radial 5mm lead spacing	EVOX RIFA	PFR5 102J630J11L4	RS: 240-4836
14	1	C17	4.7 µF	20%	50 V		Electrolytic capacitor	Cylindrical 2.5 mm lead spacing			
15	2	C18, C19	100 nF-ceramic	5%	50 V		COG Ceramic capacitor	SMD 0805			
16	1	C20	1 nF Y1	20%	250 Vac		Y1 Ceramic capacitor	Radial 9.5 mm lead spacing	CERA MITE	440LD10-AD 10PCM	RS: 214-5896
17	1	C21	100 nF	10%	630 V		polypropylene capacitor	Radial 15 mm lead spacing	EPCOS	B32652A6104K	RS: 190-8371
18	1	C22	220 pF - ceramic-lead spacing 5 mm	10%	1 kV		Ceramic disc capacitor	Radial 5mm lead spacing	Panasonic	ECKA3A221KB P	RS: 473-0373
19	1	C25	Not mounted								
20	3	D7,D11, D12	BAT46		150 mA		Small signal Schottky diode	SMD SOD-323	STMicro-electronics	BAT46JFILM	
21	1	D2	STTH1L06				Ultrafast high voltage rectifier	DO-41	STMicro-electronics	STTH1L06	
22	4	D3,D4, D5,D6	GF1M-1A		1000 V 1 A		Rectifier diode	SMD DO214BA			RS: 269-451
23	2	D8, D13	LL4148		75 V 150 mA		Switching diode	SMD SOD-80			
24	1	D9	16 V	5%	16 V	500 mW	Zener diodes	SMD SOD-123			RS: 447-1838
25	1	D10	1N4007		1000V 1 A		Rectifier diode	DO-41			
26	1	F1	3,15 A		250 V		TR5 quick acting submin PCB F fuse	RADIAL			RS: 226-6549
27	1	J1	CON3				3 way screw terminal block 7.5 mm pitch	THT 7.5 mm lead spacing			RS: 548-7317
28		Lamp, Lamp2	T8 Lamp1-58 W		250V		4 pins PCB terminal strip	THT 5 mm lead spacing	WAGO (www. wago.it)	739-104	

Table 5. Bill of material (continued)

Item	Qty	Ref.	Part/value	Tolerance (%)	Voltage - current	Watt	Technology information	Package footprint	Manu-facturer	Manufacturer code	RS/ distrelec /other code
29	1 Note(1)	LPFC1	0.8 mH								
30	1	LPFC2	2x39 mH/0.7 A				Common mode choke		EPCOS	B82732R2701B 030	
31	2 Note(1)	L1, L2	1.8 mH +/- 5%	5%							
32	3	Q5, Q6, Q8	BC847		100 mA		NPN transistor	SMD SOT-23			
33	2	Q2, Q4	STD8NM60 N		600 V 7 A		MDmesh™ Power MOSFET	SMD DPAK	STMicro-electronics	STD8NM60N	
34	1	Q3	STD6NK50Z		500 V 6 A		Supermesh MOSFET	SMD DPAK	STMicro-electronics	STD6NK50Z	
35	1	Q7	X0205MA		600 V 0.050 mA		SCRs	TO92	STMicro-electronics	X0205MA	
36	2	R3, R4	560 kΩ	1%		1/4 W	Metal film resistor	SMD 1206			
37	1	R5,	1 MΩ	1%		1/4 W	Metal film resistor	SMD 1206			
38	2	R7, R12	910 kΩ	1%		1/4 W	Metal film resistor	SMD 1206			
39	2	R6, R11	1.5 MΩ	1%		1/4 W	Metal film resistor	SMD 1206			
40	1	R8	16 kΩ	1%		1/8 W	Metal film resistor	SMD 0805			
41	1	R9	390 kΩ	1%		1/4 W	Metal film resistor	SMD 1206			
42	1	R10	15 kΩ	5%		1/4 W	Carbon film resistor	axial			
43	1	R13	30 KΩ	1%		1/8 W	Metal film resistor	SMD 0805			
44	1	R14	20 kΩ	1%		1/8 W	Metal film resistor	SMD 0805			
45	1	R15	1.2 MΩ	1%		1/8 W	Metal film resistor	SMD 0805			
46	1	R16	240 kΩ	1%		1/8 W	Metal film resistor	SMD 0805			
47	1	R17	20//11 kΩ - *parallelo-*	1%		1/4 W	Metal film resistor	SMD 1206			
48	1	R18	18 kΩ	1%		1/4 W	Metal film resistor	SMD 1206			
49	1	R19	13 kΩ	1%		1/4 W	Metal film resistor	SMD 1206			
50	2	R20, R23	62 Ω	1%		1/8 W	Metal film resistor	SMD 0805			
51	2	R21, R48	10 Ω	1%		1/8 W	Metal film resistor	SMD 0805			
52	1	R29	10 Ω	1%		1/4 W	Metal film resistor	SMD 1206			

Table 5. Bill of material (continued)

Item	Qty	Ref.	Part/value	Tolerance (%)	Voltage - current	Watt	Technology information	Package footprint	Manu-facturer	Manufacturer code	RS/ distrelec /other code
53	2	R22, R31	0.33 Ω	1%		1W	Precision wire resistors	axial			Distrele: 720643
54	1	R24	1.8 MΩ	1%		1/4 W	Metal film resistor	SMD 1206			
55	1	R25	1.6 kΩ	1%		1/4 W	Metal film resistor	SMD 1206			
56	1	R26	10 kΩ	1%		1/4 W	Metal film resistor	SMD 1206			
57	4	R27,R3, R37,R41	56 kΩ	5%		1/4 W	Carbon film resistor	axial			
58	1	R50	56 kΩ	1%		1/8 W	Metal film resistor	SMD 0805			
59	3	R32,R33, R52	0 Ω jumper					SMD 1206			
60	2	R53, R54	0 Ω jumper					SMD 0805			
61	2	R34,R35	180 kΩ	1%		1/4 W	Metal film resistor	SMD 1206			
62	2	R36,R40	68 kΩ	5%		1/4 W	Carbon film resistor	axial			
63	1	R46	470 kΩ	1%		1/8 W	Metal film resistor	SMD 0805			
64	2	R47,R49	330 kΩ	1%		1/8 W	Metal film resistor	SMD 0805			
65	1	R51	2 kΩ	1%		1/8 W	Metal film resistor	SMD 0805			
66	1	R55	470 Ω	1%		1/8 W	Metal film resistor	SMD 0805			
67	1	R56	18 kΩ	1%		1/4 W	Metal film resistor	SMD 1206			
68	1	U1	L6585D				Combo IC for PFC and ballast control	SMD SO-20	STMicro-electronics	L6585D	
69	1	U2	TSM101				Voltage and current controller	SMD SO-8	STMicro-electronics	TSM101AIDT	
70	15	JUMP	Insulate wire- jump Note(2)	Wire 0.6 mm			Wire 0.6 mm				
71	4	Spacer	Spacer/ distanziatori	10 mm			Nylon				

1. Nostra Fornitura max 50 pcs
2. The wire-jump must be insulated

7 Revision history

Table 6. Document revision history

Date	Revision	Changes
06-Aug-2008	1	Initial release

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